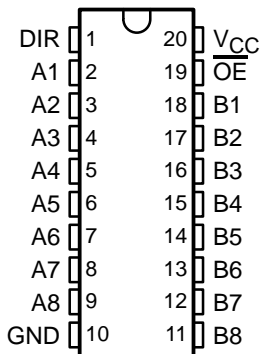


SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

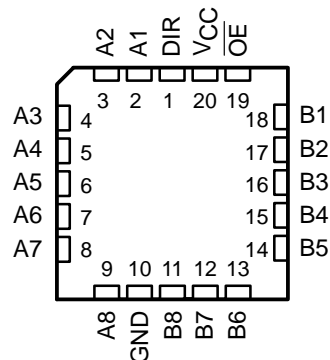
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- 4.5-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 5.5 ns at 5 V
- 3-State Outputs Drive Bus Lines Directly
- pnp Inputs Reduce dc Loading

SN54ALS245A . . . J OR W PACKAGE
SN54AS245 . . . J PACKAGE
SN74ALS245A . . . DB, DW, N, OR NS PACKAGE
SN74AS245 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|------------------|---------------|----------------|-----------------------|------------------|----------------|
| 0°C to 70°C | PDIP – N | Tube | SN74ALS245A-1N | SN74ALS245A-1N | |
| | | | SN74ALS245AN | SN74ALS245AN | |
| | | | SN74AS245N | SN74AS245N | |
| | SOIC – DW | Tube | SN74ALS245ADW | ALS245A | |
| | | | SN74ALS245ADWR | | |
| | | | Tape and reel | SN74ALS245A-1DW | ALS245A-1 |
| | | | | SN74ALS245A-1DWR | |
| | | | Tape and reel | SN74AS245DW | AS245 |
| | | | | SN74AS245DWR | |
| | SOP – NS | Tape and reel | SN74ALS245ANSR | ALS245A | |
| SN74ALS245A-1NSR | | | ALS245A-1 | | |
| SN74AS245NSR | | | 74AS245 | | |
| SSOP – DB | Tape and reel | SN74ALS245ADBR | G245A | | |
| | | CDIP – J | Tube | SNJ54ALS245AJ | SNJ54ALS245AJ |
| | | | | SNJ54AS245J | SNJ54AS245J |
| CFP – W | Tube | SNJ54ALS245AW | SNJ54ALS245AW | | |
| | | LCCC – FK | Tube | SNJ54ALS245AFK | SNJ54ALS245AFK |
| | | | | SNJ54AS245FK | SNJ54AS245FK |
| -55°C to 125°C | LCCC – FK | Tube | SNJ54ALS245AFK | SNJ54ALS245AFK | |
| | | | SNJ54AS245FK | SNJ54AS245FK | |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description/ordering information(continued)

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

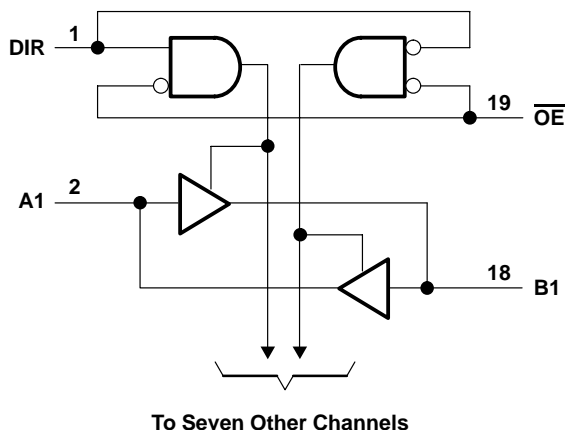
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The -1 version of the SN74ALS245A is identical to the standard version, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS245A.

FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (SN54ALS245A, SN74ALS245A) (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I : All inputs | 7 V |
| I/O ports | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 1): DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Storage temperature range | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 2)

| | | SN54ALS245A | | | SN74ALS245A | | | UNIT | | |
|----------|--------------------------------|-------------|-----|-----|-------------|-----|-----|------|----|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V | | |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V | | |
| V_{IL} | Low-level input voltage | 0.7 | | | 0.8 | | | V | | |
| I_{OH} | High-level output current | -12 | | | -15 | | | mA | | |
| I_{OL} | Low-level output current | 12 | | | 24 | | | mA | | |
| | | | | | 48† | | | | | |
| T_A | Operating free-air temperature | -55 | | | 125 | | | 0 | 70 | °C |

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54ALS245A | | | SN74ALS245A | | | UNIT | |
|---------------------|----------------|--|--------------------------|------|-----|--------------|------|-----|---------------|----|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | -1.5 | | | -1.5 | | | V | |
| V_{OH} | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V | |
| | | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$ | 2.4 | 3.2 | | 2.4 | 3.2 | | | |
| | | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$ | 2 | | | | | | | |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -15\text{ mA}$ | | | 2 | | | V | |
| | | | $I_{OL} = 12\text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | | | |
| | | | $I_{OL} = 24\text{ mA}$ | | | | 0.35 | 0.5 | | |
| I_I | Control inputs | $V_{CC} = 5.5\text{ V}$ | $V_I = 7\text{ V}$ | | | 0.1 | | | mA | |
| | A or B ports | | $V_I = 5.5\text{ V}$ | | | 0.1 | | | | |
| I_{IH} | Control inputs | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | 20 | | | 20 | | | μA | |
| | A or B ports§ | | 20 | | | 20 | | | | |
| I_{IL} | Control inputs | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | -0.1 | | | -0.1 | | | mA | |
| | A or B ports§ | | -0.1 | | | -0.1 | | | | |
| I_{O}^{\parallel} | | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -20 | -112 | -30 | -112 | | mA | | |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$ | Outputs high | | | 30 | 48 | 30 | 45 | mA |
| | | | Outputs low | | | 36 | 60 | 36 | 55 | |
| | | | Outputs disabled | | | 38 | 63 | 38 | 58 | |

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

‡ All typical values are $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-----------------|-------------|--|-----|-------------|-----|------|
| | | | SN54ALS245A | | SN74ALS245A | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | B or A | 1 | 19 | 3 | 10 | ns |
| t _{PHL} | | | 1 | 14 | 3 | 10 | |
| t _{PZH} | \overline{OE} | A or B | 2 | 30 | 5 | 20 | ns |
| t _{PZL} | | | 2 | 29 | 5 | 20 | |
| t _{PHZ} | \overline{OE} | A or B | 2 | 14 | 2 | 10 | ns |
| t _{PLZ} | | | 2 | 30 | 4 | 15 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (SN54AS245, SN74AS245) (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V _{CC} | 7 V |
| Input voltage, V _I : All inputs | 7 V |
| I/O ports | 5.5 V |
| Package thermal impedance, θ _{JA} (see Note 1): DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Storage temperature range | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

| | | SN54AS245 | | | SN74AS245 | | | UNIT |
|-----------------|--------------------------------|-----------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | | | –12 | | | –15 | mA |
| I _{OL} | Low-level output current | | | 48 | | | 64 | mA |
| T _A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54AS245 | | SN74AS245 | | UNIT | |
|------------|---|--------------------------|----------------------|-------|--------------|-------|------|---------------|
| | | | MIN | TYP† | MAX | MIN | | TYP† |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | -1.2 | | -1.2 | | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V | |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -3\text{ mA}$ | 2.4 | 3.2 | 2.4 | 3.2 | | |
| | | $I_{OH} = -12\text{ mA}$ | 2 | | | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | 0.3 0.55 | | | | V | |
| | | $I_{OL} = 64\text{ mA}$ | | | 0.35 0.55 | | | |
| I_I | Control inputs | $V_{CC} = 5.5\text{ V}$ | $V_I = 7\text{ V}$ | 0.1 | | 0.1 | | mA |
| | A or B ports | | $V_I = 5.5\text{ V}$ | 0.1 | | 0.1 | | |
| I_{IH} | Control inputs | $V_{CC} = 5.5\text{ V}$ | $V_I = 2.7\text{ V}$ | 50 | | 20 | | μA |
| | A or B ports‡ | | | 70 | | 70 | | |
| I_{IL} | Control inputs | $V_{CC} = 5.5\text{ V}$ | $V_I = 0.4\text{ V}$ | -0.5 | | -0.5 | | mA |
| | A or B ports‡ | | | -0.75 | | -0.75 | | |
| I_O^{\S} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | | -50 | -150 | -50 | -150 | mA | |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | | Outputs high | 62 | 97 | 62 | 97 | mA |
| | | | Outputs low | 95 | 143 | 95 | 143 | |
| | | | Outputs disabled | 79 | 123 | 79 | 123 | |

† All typical values are $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}^{\parallel}$ | | | | UNIT |
|-----------|-----------------|-------------|--|------|-----------|-----|------|
| | | | SN54AS245 | | SN74AS245 | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 2 | 9.5 | 2 | 7.5 | ns |
| t_{PHL} | | | 2 | 9 | 2 | 7 | |
| t_{PZH} | \overline{OE} | A or B | 2 | 11 | 2 | 9 | ns |
| t_{PZL} | | | 2 | 10.5 | 2 | 8.5 | |
| t_{PHZ} | \overline{OE} | A or B | 2 | 7.5 | 2 | 5.5 | ns |
| t_{PLZ} | | | 2 | 12 | 2 | 9.5 | |

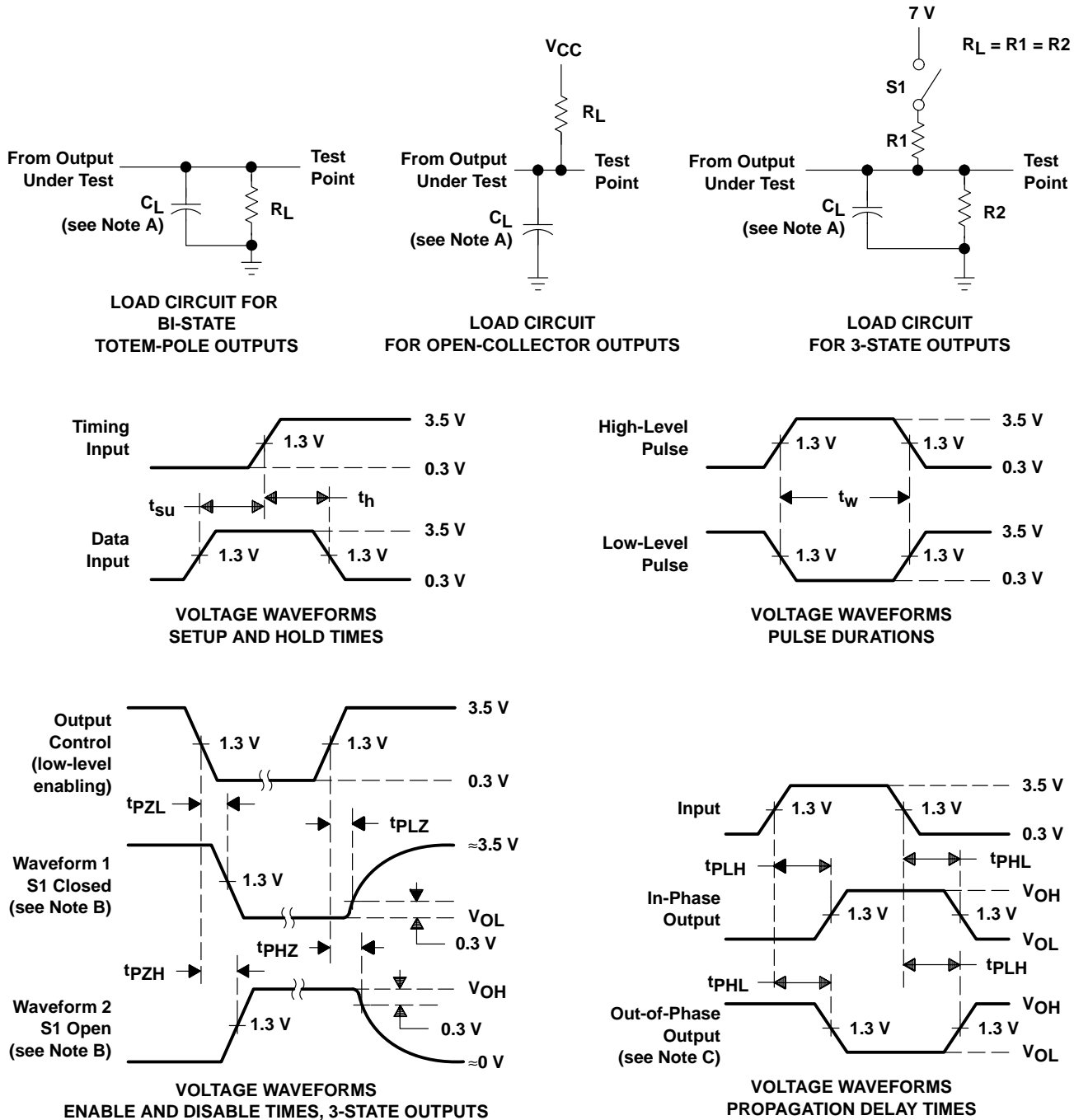
[¶] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 84030012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84030012A SNJ54ALS 245AFK | Samples |
| 8403001RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403001RA SNJ54ALS245AJ | Samples |
| 8403001SA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403001SA SNJ54ALS245AW | Samples |
| SN54ALS245AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS245AJ | Samples |
| SN54AS245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54AS245J | Samples |
| SN74ALS245A-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A-1 | Samples |
| SN74ALS245A-1DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A-1 | Samples |
| SN74ALS245A-1DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A-1 | Samples |
| SN74ALS245A-1DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A-1 | Samples |
| SN74ALS245A-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS245A-1N | Samples |
| SN74ALS245A-1NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS245A-1N | Samples |
| SN74ALS245A-1NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A-1 | Samples |
| SN74ALS245ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74ALS245ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | G245A | Samples |
| SN74ALS245ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | G245A | Samples |
| SN74ALS245ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74ALS245ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| SN74ALS245ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74ALS245ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74ALS245ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74ALS245AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS245AN | Samples |
| SN74ALS245AN3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74ALS245ANE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS245AN | Samples |
| SN74ALS245ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74ALS245ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS245A | Samples |
| SN74AS245DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS245 | Samples |
| SN74AS245DWR | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS245DWRE4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS245DWRG4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS245N | Samples |
| SN74AS245NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS245 | Samples |
| SNJ54ALS245AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84030012A SNJ54ALS 245AFK | Samples |
| SNJ54ALS245AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403001RA SNJ54ALS245AJ | Samples |
| SNJ54ALS245AW | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403001SA SNJ54ALS245AW | Samples |
| SNJ54AS245FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54AS 245FK | Samples |
| SNJ54AS245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54AS245J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 :

● Catalog: [SN74ALS245A](#), [SN74AS245](#)

● Military: [SN54ALS245A](#), [SN54AS245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS245A-1DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ALS245A-1NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74ALS245ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS245ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ALS245ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74AS245NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS245A-1DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS245A-1NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS245ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ALS245ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS245ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AS245NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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